Swathi Changalarayappa

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OBJECTIVE

Looking for an internship in the field of VLSI design/verification or computer architecture for Summer 2018
MS thesis in High Performance Network on Chips. Part of High performance computing laboratory, Texas A&M University

EDUCATION

TEXAS A&M UNIVERSITY

MS in Computer Engineering
May 2019 | College Station, TX
Cum. GPA: 4.0 / 4.0

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL

BTech in Electronics and Communication Engineering
May 2014 | Surathkal, India
Cum. GPA: 8.33 / 10.0

COURSEWORK

GRADUATE

Computer Architecture
Microprocessor Systems Design
Digital Integrated Circuits Design
Computer Arithmatic Unit Design
Analysis of Algorithms
Hardware Security

UNDERGRADUATE

Digital system design
Linear integrated circuits
VLSI design
Logic synthesis and techniques
VLSI design and automation

SKILLS

PROGRAMMING

Verilog • VHDL • C • C++ •
Perl • TCL • Python

TOOLS

Cadence NCSIM • Magillem •
Spyglass Atrenta • Autogen • MATLAB

PROFESSIONAL EXPERIENCE

TEXAS INSTRUMENTS | Design Engineer

July 2014 – July 2017 | Bangalore, India

Design and Verification

- Designed instruction cache block in Verilog by interacting with architects and other design groups
- Performed CPF based low power functional verification and coverage analysis at RTL and gate level verification of SOC, released to production
- Designed glue-logic using verilog RTL, enabling expected functionality between IPs at SOC level
- Gained expertise in IPXACT 1685 standards while integrating IPs using Magillem tool
- Achieved high quality SOC RTL handoff to synthesis team using spyglass Lint tool
- Performed logic equivalence check between RTL and synthesis/post-layout netlists achieving zero bugs

Methodology Development and Improvement

- Verified isolation correctness using checkers for low power designs leading to zero isolation bugs on production chip using perl scripting
- Identified automated checks to enable quality IP RTL handoff to SOC

Architecture

- Analyzed architecture of instruction cache to improve performance by 21% for industrial benchmarks Coremark and Dhrystone
- Estimated RTL based power using Cadence Joules to determine power/performance trade-off for cache configurations

TEXAS INSTRUMENTS | Intern

May 2013 – July 2013 | Bangalore, India

- Improved simulation time by 40% by performing Checkpoint simulation at SOC, method of creating snapshot using Cadence NCSIM simulator

ACADEMIC PROJECTS

Perceptron based cache reuse prediction for LL cache in C++
November 2017 | Texas A&M University
Implemented dead block predictor for last level caches. Speedup achieved: 6.4% over LRU. The algorithm learns from few sampled sets and generalizes over entire cache to save area and power.

ITTAGE - Indirect branch predictor in C++
October 2017 | Texas A&M University
Implemented ITTAGE to predict indirect branch targets improving performance by 93%. Enhanced the original implementation to achieve an additional speed up of 5.3%

Hardware Software Co-design
November 2017 | Texas A&M University
Developed a device driver in Linux to decode and display IR signal using Xilinx FPGA

Elevator design on Spartan FPGA
November 2012 | NITK Surathkal
Realized elevator control system for 4 floors with power conservation and safety features on Spartan FPGA using state machines